PARVATHANENI BRAHMAYYA
SIDDHARTHA COLLEGE OF ARTS & SCIENCE
Autonomous
Siddhartha Nagar, Vijayawada–520010
Re-accredited at 'A+' by the NAAC

23IOMIL121: Digital Electronics

Offered to : All UG Programs

Course Type: Minor -1 (Core -TH)

Year of Introduction: 2023-24 **Year of offering: 2023 - 2024**

Semester: II 60 Hrs **Credits: 3**

Couse Outcomes: At the end of this course, students should be able to:

Course Outcome NO	Outcome	Mapping to
CO1	Remember the binary number theory of digital circuits	PO2
CO2	Understand the concepts of Boolean algebra and have knowledge to analyze and design combinational systems using standard gates and minimization methods (such as karnaugh maps)..	PO2
CO3	Apply design various logical inputs of different IC-logic families	PO1
CO4	Analyze design flip-flops and latches for sequential systems composed of standard sequential modules, such as counters and registers	PO6
CO5	: Evaluate combinational systems composed of standard combinational modules, such as multiplexers and decoders and understand various data manipulation circuits	PO7

CO-PO MATRIX								
	CO-PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**
23IOMIL121	**CO1**		2					
	CO2		3					
	CO3	2						
	CO4						3	
	CO5							2

UNIT-I- (12HRS)
NUMBER SYSTEM AND CODES:
Decimal, Binary, Hexadecimal, Octal, BCD, Conversions, Complements (1‘s,2‘s, 9‘s and10‘s), Addition, Subtraction, Grey, Excess-3, inter Code conversion between number system.

UNIT-II-(12HRS)
BOOLEAN ALGEBRA AND THEOREMS:
Boolean Theorems, De Morgan‘s laws. Digital logic gates, Multilevel NAND & NOR gates. Standard representation of logic functions (SOP and POS), Minimization Techniques (Karnaugh Map Method: 4 variables), don‘t care condition.

Unit-III-(12HRS)
IC LOGIC FAMILIES:
Digital Logic Families: Characteristics of logic families AND DTL, ECL, RTL, TTL and CMOS logic circuits- Inverter, NAND , NOR. Bi- CMOS Inverter and its characteristics.

UNIT-IV-(12HRS)
COMBINATIONAL DIGITAL CIRCUITS:
Adders: Half & full adder, Subtractor – Half and Full Subtractor, Parallel binary adder, Magnitude Comparator, Multiplexers (2:1, 4:1)) and De-multiplexers (1:2, 4:1) , Encoder(8- line-to-3-line) and Decoder (3-line-to-8-line).

UNIT-V-(12HRS)
SEQUENTIAL DIGITAL CIRCUITS:
Flip -Flops: S-RFF,J-KFF,T and D type FFs , Master –Slave FFs ,Excitation tables ,Registers: shift left register, shift rightregister,Counters-Asynchronous-Mod16, Mod-10,Mod-8, Downcounter,Synchronous-4-bit&Ring counter.

TEXTBOOKS:
1. M.MorrisMano, ―Digital Design― 3rdEdition, PHI, New Delhi.
2 Fundamentals of Digital Circuits by Anand Kumar

ReferenceBooks:
1. Herbert Tau band Donald Schilling. ―Digital Integrated Electronics‖ .McGraw-Hill.1985.
2. S.K.Bose.―DigitalSystems‖.2/e. New Age International.1992.

Course Delivery method: Face-to-face / Blended

Course has focus on: **F**oundation and **S**kill Development

Websites of Interest: https://www.javatpoint.com/, https://www.geeksforgeeks.org/

Co-curricular Activities: Assignments, PPT’s, Mini projects.

PARVATHANENI BRAHMAYYA
SIDDHARTHA COLLEGE OF ARTS & SCIENCE
Autonomous
Siddhartha Nagar, Vijayawada–520010
Re-accredited at 'A+' by the NAAC

Model Question Paper

23IOMIL121DIGITAL ELECTRONICS **Maximum Marks: 70M**

Time: 3 Hours **Pass Minimum: 28M**

SECTION – A

Answer the following: **5 x 4 = 20 M**

1. (a)Write about Excess-3 code with example (**C01-L1)**

(or)

(b)Convert the following decimal number (245) in to binary. **(C01-L1)**

2. (a)Explain about universal gates (**C02-L1)**

(or)

(b)Explain about multilevel NAND gate (**C02-L1)**

3. (a) Write about the characteristics of logic families. **(C03-L2)**

(or)

(b) Explain about ECL logic family (**C03-L2)**

4. (a) Discuss about magnitude comparator in brief. (**C04-L1)**

(or)

(b)Explain about decoder and encoder with one example each. (**C04-L1)**

5. a)Explain the construction and working of D-Flip-flop. (**C05-L2)**

(or)

b)Discuss about Shift registers in brief. **(C05-L2)**

Section – B

Answer the following: **5 x 10 = 50 M**

6.(a)Explain about rules of 1's compliment and 2's compliment method.-(**co1)-(L1)**

(or)

(b) Convert the following grey code to binary vice-versa.

(1)11101 (2)100110—(**co1-L1)**

7.(a)Explain briefly about canonical and standard form of Boolean algebra.**(c02-L2)**

(or)

(b)Simplify the following functions in sum of products using K-map and draw their implementation.

(i)F (A, B, C, D) =∑ (7, 13, 14, 15)

(ii)F(w,x,y,z)=∑(1,3,7,11,15)+d∑(0,2,5) **-(c02-L2)**

8. (a) Discuss briefly about CMOS NOR gate with their truth tables. (**C03-L2)**

(or)

(b)Discuss about the construction and working of TTL NAND gate and Characteristics.(**Co3-L2)**

9. a)Explain the construction and working of HALF adder and FULL adder with their logic circuits. **(C04-L1)**

(or)

b)Explain the construction and working of HALF sub tractor and FULL sub tractor with their logic circuits. **(C04-L1)**

10.(a) Explain the operation of JK-Flip-flop and draw the timing diagram **C05-(L2)**

(or)

(b) Define counter and Explain briefly about ripple counter. **C05-(L2)**

***