PARVATHANENI BRAHMAYYA
SIDDHARTHA COLLEGE OF ARTS & SCIENCE
Autonomous
Siddhartha Nagar, Vijayawada–520010
Re-accredited at 'A+' by the NAAC

23IOMIP121: Digital Electronics Lab Offered to : All UG Programs

Semester – II Minor -1 (P) **Credits: 01**

CO1 : Remember the binary number theory of digital circuits PO3
CO2 : To verify the truth table of Digital IC logic gates.PO1
CO3 : Apply design various logical inputs of different IC- logic familiesPO7
C04: To verify the truth table of Flip-flops. PO1
C05: To verify the truth table of ADDERS.PO1

CO-PO MATRIX								
	CO-PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**
23IOMIP121	**CO1**			2				
	CO2	2						
	CO3							3
	CO4	3						
	CO5	3						

L=1 M =2 H =3

LAB LIST:

1. Verification of IC-logic gates
2. Verification of De-Morgan's laws
3. Verify one bit comparator
4. Realization of basic gates using Universal gates (NAND & NOR gates)
5. Verify Half adder and full adder using gates
6. Verify Half subtractor and full subtractor using gates.
7. Verify the truth table of RS-F/F using NAND gates
8. Verify the truth table of JK-F/F using NAND gates
9. 4-bit binary parallel adder and subtractor using IC 7483

Lab experiments are to be done on breadboard and simulation software (using Multisim) and output values are to be compared and justified for variation.

LAB MANUAL ARE SUPPLIED BY DEPARTMENT

Question Paper Pattern for Core Lab Courses

SEE (LAB) Model Question Paper

23IOMIP121 Offered to: BCA, B.Sc.-AI

Max.Marks: 35 Max.Time: 3Hours

Pass. Min: 14

(A) Evaluation Procedure Max. Marks: 30

Each and every student must complete 10 practicals at the time of lab the student has to select one of the practical and perform practical on bread board using components.

1. Aim, Apparatus, Circuit diagram, Tabular form-	10m
2. Experiment -	10m
3. Result-	5m
4. Viva-	5m
5. Record-	5m
(B) Continuous Assessment:	15 MARKS
TOTAL : (A)+(B) =	50MARKS