PARVATHANENI BRAHMAYYA
SIDDHARTHA COLLEGE OF ARTS & SCIENCE
Autonomous
Siddhartha Nagar, Vijayawada–520010
Re-accredited at 'A+' by the NAAC

Course Code				**23ELMAP231**			
Title of the Course				**Digital Electronics lab**			
Offered to: (Programme/s)				B.Sc. (H)-Electronics			
L	**0**	**T**	**0**	**P**	**2**	**C**	**1**
Year of Introduction:	**2024-25**			**Semester:**			**3**
Course Category:	Major			**Course Relates to:**	Global		
Year of Revision:	**N/A**			**Percentage:**	**N/A**		
Type of the Course:				Skill development			
Crosscutting Issues of the Course :							
Pre-requisites, if any				**Basic knowledge on Basic Electronics.**			

Course Description:

In this lab, we explored fundamental concepts of digital electronics, focusing on logic gates, combinational and sequential circuits. We constructed and tested basic gates (AND, OR, NOT, NAND, NOR, XOR) using integrated circuits. Additionally, we built a 4-bit binary adder to demonstrate combinational logic and a D flip-flop to illustrate sequential logic. Measurements were taken with an oscilloscope to verify the timing and functionality of each circuit. The lab emphasized the importance of accurate wiring and timing analysis. Through these experiments, we gained practical insights into designing and troubleshooting digital systems, which are crucial for modern electronics and computing applications.

Course Aims and Objectives:

S.NO	COURSE OBJECTIVES
1	Understand the operation and application of basic logic gates (AND, OR, NOT, NAND, NOR, XOR).
2	Design and implement combinational circuits such as adders, multiplexers, and decoders
3	Construct and analyze sequential circuits like flip-flops, counters, and registers.
4	Develop skills in reading and creating digital circuit schematics.
5	Apply digital logic principles in practical problem-solving scenarios.

Course Outcomes

At the end of the course, the student will be able to…

CO NO	COURSE OUTCOME	BTL	PO	PSO
CO1	Understand and describe the functions of basic logic gates (AND, OR, NOT, NAND, NOR, XOR)	K2	2	1
CO2	Create and analyze combinational circuits such as adders, multiplexers, and decoders,	K4	2	1
CO3	Build and test sequential circuits like flip-flops, counters, and registers, and understand their role in digital systems.	K5	2	1
CO4	Develop the ability to interpret and produce accurate digital circuit diagrams.	K5	2	1
CO5	Enhance skills in identifying and resolving issues in digital circuits through systematic testing and analysis.	K5	2	1

For BTL: K1: Remember; K2: Understand; K3: Apply; K4: Analyze; K5: Evaluate; K6: Create

CO-PO MATRIX									
CO NO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2
CO1		2						2	
CO2		3						3	
CO3		3						3	
CO4		2						2	
CO5		2						2	

Use the codes 3,2,1 for High, Moderate and Low correlation Between CO-PO-PSO respectively

Course Structure

This lab list covers the key areas of a Digital Electronics lab course, providing hands-on practice with using Bread board and digital IC's and multimeter.

unit 2:

Experiment 1: Boolean Theorems and De Morgan's Laws

- **Objective:** Understand and verify Boolean theorems and De Morgan's laws.
- **Theory:** Discuss fundamental Boolean theorems and De Morgan's laws for simplification of Boolean expressions.
- **Procedure:**
    1. Simplify given Boolean expressions using Boolean theorems.
    2. Verify the simplified expressions by constructing corresponding logic circuits.
    3. Apply De Morgan's laws to given Boolean expressions and simplify.
    4. Construct and test circuits to verify De Morgan's laws.
- **Report:** Document given expressions, simplification steps, circuit diagrams, and test results.

Experiment 2: Digital Logic Gates

- **Objective:** Understand the function of basic digital logic gates.
- **Theory:** Introduction to AND, OR, NOT, NAND, NOR, XOR, and XNOR gates.
- **Procedure:**
    1. Construct basic logic gates using ICs or discrete components.

2. Verify their truth tables by applying all possible input combinations.
- **Report:** Include circuit diagrams, truth tables, and observations.

Experiment 3: Multilevel NAND and NOR Gates

- **Objective:** Design and implement multilevel NAND and NOR gate circuits.
- **Theory:** Explain how any Boolean function can be implemented using only NAND or NOR gates.
- **Procedure:**
  1. Design given Boolean expressions using only NAND gates.
  2. Design the same expressions using only NOR gates.
  3. Construct the circuits and verify their functionality.
- **Report:** Provide Boolean expressions, circuit diagrams, and test results for both NAND and NOR implementations.

Unit 4: Experiment 4: **Half Adder**

Objective: Understand the basic operation of a half adder.

- **Components:** XOR gate, AND gate.
- **Circuit Design:** Construct a half adder circuit.
- **Testing:** Verify the output for different combinations of input values (A, B).
- **Measurements:** Measure output for sum and carry.

Activity: Build the half adder circuit and test its functionality.

Experiment 5: Full Adder

Objective: Learn about the full adder which includes carry-in functionality.

- **Components:** Two XOR gates, two AND gates, one OR gate.
- **Circuit Design:** Construct a full adder circuit.
- **Testing:** Verify the output for all possible input combinations (A, B, Cin).
- **Measurements:** Measure the sum and carry outputs.

Activity: Build the full adder circuit and test it with different inputs.

Experiment 6:. Half Subtractor

Objective: Understand the operation of a half subtractor.

- **Components:** XOR gate, AND gate, NOT gate.
- **Circuit Design:** Construct a half subtractor circuit.
- **Testing:** Verify the output for different combinations of input values (A, B).
- **Measurements:** Measure output for difference and borrow.

Activity: Build the half subtractor circuit and analyze its performance.

Experiment 7: Full Subtractor

Objective: Learn about the full subtractor, which includes borrow-in functionality.

- **Components:** Two XOR gates, two AND gates, two OR gates, one NOT gate.
- **Circuit Design:** Construct a full subtractor circuit.
- **Testing:** Verify the output for all possible input combinations (A, B, Bin).
- **Measurements:** Measure the difference and borrow outputs.

Activity: Build the full subtractor circuit and test it.

Experiment 8: Magnitude Comparator

Objective: Compare two binary numbers and determine their magnitude relationship.

- **Components:** Combination of logic gates.
- **Circuit Design:** Construct a 4-bit magnitude comparator.
- **Testing:** Verify the comparator's output for different 4-bit input pairs.
- **Measurements:** Measure the outputs for equality, greater than, and less than conditions.

Activity: Build a 4-bit magnitude comparator and analyze its functionality.

Unit 5:

Experiment 9: S-R Flip-Flop (Set-Reset)

Objective: Understand the basic operation and characteristics of the S-R flip-flop.

- **Components:** NAND or NOR gates.
- **Circuit Design:** Construct an S-R flip-flop using NAND or NOR gates.
- **Testing:** Verify the operation for different combinations of Set (S) and Reset (R) inputs.
- **Measurements:** Measure setup time, hold time, and propagation delay.

Activity: Build and test an S-R flip-flop. Record the truth table and timing diagrams.

Experiment 10: J-K Flip-Flop

Objective: Learn about the J-K flip-flop and its toggling behavior.

- **Components:** Logic gates or JK flip-flop IC (e.g., 7476).
- **Circuit Design:** Construct a J-K flip-flop.
- **Testing:** Verify the operation for different combinations of J, K, and clock inputs.
- **Measurements:** Measure setup time, hold time, and propagation delay.

Activity: Build and test a J-K flip-flop. Analyze how the flip-flop toggles on different input conditions.

Experiment 11: D Flip-Flop (Data or Delay)

Objective: Understand the operation of the D flip-flop.

- **Components:** D flip-flop IC (e.g., 7474) or constructed using logic gates.
- **Circuit Design:** Construct a D flip-flop.
- **Testing:** Verify the operation for different Data (D) and clock inputs.
- **Measurements:** Measure setup time, hold time, and propagation delay.

Activity: Build and test a D flip-flop. Record how data is latched on the clock edge.

Lab Manual:
Supplied by the Department

References:

1. [Reference 1 - Author(s), Year of Publication, Title, Edition, Publisher]
2. [Reference 2 - Author(s), Year of Publication, Title, Edition, Publisher]

LAB EXAMINATION PATTERN

23ELMAP231: Digital Electronics Lab Semester: III MAX Marks:35M

Time:3Hrs

(A) SEE Evaluation Procedure

1. For Aim, Apparatus, circuit diagram, Flow chart	**5M**
2.For Observation table, formulas, Program	**5M**
3. Experiment Procedure and Execution	**10M**
4.Output of Experiment	10M
5. Practical Record	**2M**
6. Viva voce	**3M**

(B) CONTINUOUS ASSESMENT(Internal) 15 MARKS

15 marks for the continuous assessment (Day to day work in the laboratory shall be evaluated for 15 marks by the concerned laboratory teacher based on the regularity/ record/viva). Laboratory teachers are mandated to ensure that every student completes 80%-90% of the lab assessments.

TOTAL: (A)+(B) = 50 MARKS